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Docket No.: 01 P 11902 US
INTECH 3.0-013
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Vollrath et al.

Application No.: 09/967,008

Group Art Unit: 2185

Filed: September 28, 2001

Examiner: Not Yet Assigned

For: MEMORY AND METHOD FOR EMPLOYING
-A CHECKSUM FOR ADDRESSES OF
REPLACED STORAGE ELEMENTS

Commissioner for Patents
Washington, DC 20231

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INFORMATION DISCLOSURE STATEMENT

Dear Sir:

It is respectfully requested that the information listed on the enclosed form be made of record and considered with respect to the above-referenced U.S. patent application. A copy of each piece of information is enclosed. Submission of the present Information Disclosure Statement should not be taken as an admission that the cited information is legally available prior art or that the same are pertinent or material.

This Information Disclosure Statement is being filed before a first Office Action on the merits and, therefore, no fee is believed due. In the event that any fee is due in connection with the present Information Disclosure Statement, the Commissioner is hereby authorized to charge the same to our Deposit Account No. 12-1095.

Dated: February 26, 2002

Respectfully submitted

By

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I hereby certify that this correspondence is being deposited with the U.S. Postal Service with sufficient postage as First Class Mail, in an envelope addressed to: Commissioner for Patents, Washington, DC 20231, on the date shown below.

Dated: February 26, 2002

Signature:

Matthew B. Dernier
(Matthew B. Dernier)



Sheet 1 of 1

Form PTO-1449 (REV. 8-83)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. 01 P 11902 US INTECH 3.0-013	SERIAL NO. 09/967,800
INFORMATION DISCLOSURE CITATION <i>(Use several sheets if necessary)</i>		APPLICANT Joerg Vollrath	EXAMINER Not Yet Assigned.
		FILING DATE September 28, 2001.	GROUP 2185

U. S. PATENT DOCUMENTS

Examiner INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE APPROPRIATE
							RECEIVED
							MAR 12 2002
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FOREIGN PATENT DOCUMENTS

	REF	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
							YES
							NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

A	Joerg Vollrath and Randall Rooney, "Pseudo Fail Bit Map Generation for RAMs during Component Test and Burn-In in a Manufacturing Environment," Test Conference, 2001. Proceedings. Int'l, IEEE, pp. 768-775, (Oct. 30 – Nov. 1, 2001).
B	Jorg Vollrath, Ulf Lederer, and Thomas Hladschik, "Compressed Bit Fail Maps for Memory Fail Pattern Classification," European Test Workshop, 2000. Proceedings. IEEE, pp. 125-130, (May 23-26, 2000).
C	U.S. Patent Application No. 09/455,855, filed December 7, 1999, entitled "Efficient Bit Fail Map Compression Strategy".
D	U.S. Patent Application No. 09/931,125, filed August 16, 2001, entitled "Pseudo Fail Bit Map Generation For RAMs During Component Test and Burn-In In A Manufacturing Environment".

EXAMINER	DATE CONSIDERED
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EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.